Control of 3-Leg VSC Based 3-Phase 4-Wire DSTATCOM using Modified Instantaneous Symmetrical Component Theory

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Abstract

This paper deals with a 3-leg VSC (Voltage Source Converter) with a zigzag transformer as a DSTATCOM (Distribution Static Compensator) for load compensation in 3-phase 4-wire distribution system using ISCT (Instantaneous Symmetrical Component Theory) based control algorithm which is modified for the voltage regulation and used with indirect current control technique. The DSTATCOM is controlled to compensate the reactive power, harmonics currents, the neutral current and balance the unbalanced loads in the distribution system. Simulations are performed for the various load conditions such as a reactive linear load, an unbalanced load and a non-linear load in PFC (Power Factor Correction) as well as in ZVR (Zero Voltage Regulation) modes in MATLAB environment using SIMULINK and SimPowerSystem toolbox. Extensive tests have been performed on a developed prototype of DSTATCOM to validate the control algorithm.

Keywords

DSTATCOM; Control Algorithm; Power Quality; Nonlinear Load; Load Balancing; Harmonic Compensation; Voltage Regulation; Zigzag Transformer; Neutral Current Compensation; Instantaneous Symmetrical Component Theory

Introduction

Presently, the power quality is a big issue at the load end in the distribution system. As the majority of loads in the power distribution system are linear/ nonlinear and balanced/ unbalanced or combination in nature such as adjustable speed drives in fans and pumps, variable frequency drives and power converters with poor power factor used in industries as well as in home appliances. These loads increase the burden on the system by drawing reactive power and injecting harmonics which influence the performance of other loads connected to the same utility end. Moreover, unbalanced loads cause unbalanced voltages at the utility end. The DSTATCOM (Distribution Static Compensator) is used to mitigate such power quality problems at the point of common coupling (PCC) [1-10]. A three phase four wire DSTATCOM is used to compensate the neutral current along with voltage regulation or power factor correction with harmonics elimination and load balancing. Many topologies of DSTATCOM are reported in the literature to compensate the neutral current with three phase four wire such as a 4-leg VSC (H. Akagi, 2007), three single-phase VSC (H. Akagi, 2007), 3-leg VSC with split capacitor (K. R. Padiyar, 2007), H-bridge VSC with star-hexagon-transformer (P. Jayaprakash, 2008), H-bridge VSC with star-delta transformer (B. Singh, 2008) and three-leg DTATCOM with zigzag transformer (B. Singh, 2008). The zigzag transformer is used to compensate the load neutral current by providing a path for zero sequence current. Moreover, the application of a zigzag transformer with the active compensation techniques has less complexity.

Many control techniques are reported in the literature [1-10, 17-27] to extract the reference supply currents such as IRPT (Instantaneous Reactive Power Theory) (H. Akagi,2007), SRF (Synchronous Reference Frame) theory K. R. Padiyar, 2007, PI controller based controller (B. Singh), NN (Neural Network) based adaline control scheme (B. Singh, 2011) and ISCT (Instantaneous Symmetrical Components Theory) (Arindam Ghosh, 2000) to control the DSTATCOM.

In this paper, modified ISCT (Instantaneous Symmetrical Components Theory) based control algorithm is used to control the DSTATCOM in voltage regulation without a major change in the programme and hardware of controller. As the supply currents are slow varying currents, the modified control algorithm is implemented with indirect current

control scheme to control the current of the DSTATCOM. A 3-leg VSC with a zigzag transformer as DSTATCOM is implemented with modified ISCT using dSPACE DSP (Digital Signal Processor). The DSTATCOM with the proposed modified algorithm is found capable to compensate the load harmonics currents and load balancing along with PFC (Power Factor Correction) or ZVR (Zero Voltage Regulation). The dynamic as well as steady state performances of DSTATCOM is studied for both PFC as well as ZVR modes in a 3-phase 4-wire distribution system.

System Configuration

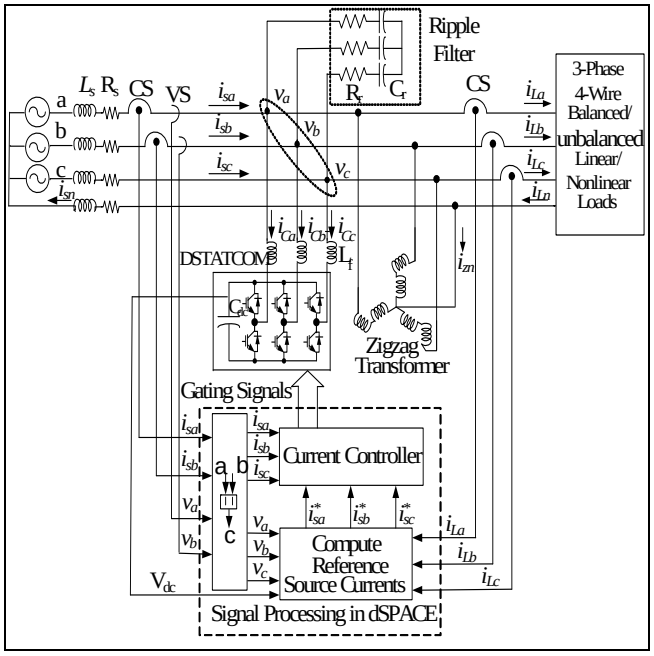


FIG. 1 CIRCUIT DIAGRAM OF HARDWARE IMPLEMENTATION OF DSTATCOM.

The basic circuit diagram of DSTATCOM connected to the three phase four wire distribution system supplying the power to a three phase four wire loads is shown in Fig. 1. Three-phase load may be a lagging/leading power factor load or an unbalanced load or a non linear load or combination of all of them. The zigzag transformer provides the path for the load neutral current. The VSC is realized using six IGBTs (Insulated Gate Bipolar Transistors) switches with anti parallel diodes and a DC capacitor. To reduce the ripples in compensating currents, the interfacing inductors are used to connect the VSC to the supply system. A RC filter is connected to the system in parallel with the load and the compensator to reduce the switching ripples in the PCC voltage injected by the fast switching of DSTATCOM. The DSTATCOM is controlled for the compensation of reactive and harmonic currents of the load to correct the power factor at AC mains or to regulate the voltage at PCC. In PFC mode, the supply currents have zero phase shifts with respect to PCC voltages. In ZVR mode, DSTATCOM injects the currents to regulate the PCC voltage at the desired reference value of voltage, but in this case, the supply currents may be leading or lagging currents depending on the power factor of load and reference PCC voltage.

Control Algorithm

The block diagram of modified control algorithm is shown in Fig. 2. PCC voltages (v_a,, v_b and v_c), supply currents (i_{sa}, i_{sb} and i_{sc}), load currents (i_{La}, i_{Lb} and i_{Lc}) and DC bus voltage (V_{dc}) of the DSTATCOM are sensed as feedback signals to extract reference supply currents. The control algorithm is based on primary objective to obtain the balanced supply currents. For that, the positive sequence quantities of the voltages and currents are considered like in conventional ISCT (Arindam Ghosh, 2000). Therefore reference supply currents are considered as:

$$i_{sa}^{*} + i_{sb}^{*} + i_{sc}^{*} = 0 \quad (1)$$

From the power factor consideration, the phase angle between v_{sa} and i_{sa} is ø then:

$$\angle\{v_a + av_b + a^2v_c\} = \angle\{i_{sa}^{*} + ai_{sb}^{*} + a^2 i_{sc}^{*}\} - \phi \quad (2a)$$

$$\tan^{-1}\{K_1/K_2\} = \tan^{-1}\{K_3/K_4\} - \phi \quad (2b)$$

where

$$K_1 = \sqrt{3/2}(v_b - v_c)\,;\; K_2 = (3/2)v_a\,;$$

$$K_3 = \sqrt{3/2}(i_{sb}^{*} - i_{sc}^{*})\,;\; K_2 = i_{sa}^{*} - i_{sb}^{*}/2 - i_{sc}^{*}/2$$

Defining $\beta = \tan\phi/\sqrt{3}$ (2c)

After solving eqns. (2a, 2b and 2c), it results in:

$$(v_b - v_c + \beta v_a)i_{sa}^{*} + (v_c - v_a + \beta v_b)i_{sb}^{*} + (v_a - v_b + \beta v_c)i_{sc}^{*} = 0 \quad (3)$$

For β=0, the supply currents are to be in phase of PCC voltages. It implies that the reactive power demand of the load is supplied by the DSTATCOM. For nonzero value of β, the source supplies/absorbs the reactive power corresponding to the β. Therefore, in this paper, β is used to regulate the voltage at PCC. The objective of the compensator is that the source must supply the load active power and the losses of the DSTATCOM in PFC mode:

$$v_a i_{sa}^{*} + v_b i_{sb}^{*} + v_c i_{sc}^{*} = p_{lavg} + p_{loss} \quad (4)$$

where p_{lavg} is filtered average load active power calculated from load power $p_l = v_a i_{La} + v_b i_{Lb} + v_c i_{Lc}$ using the moving average filter. The active load power is calculated by a moving average filter with averaging time of half cycle of the supply frequency.

p_{loss} is the loss of the DSTATCOM which should be supplied from the AC mains for the self supporting DC bus and is estimated by the PI controller over the DC bus voltage as:

$$p_{loss} = K_{pd}V_{dce} + K_{id}\int V_{dce}dt \quad (5)$$

where $V_{dce} = V_{dc}^{*} - V_{dc}$ = error in DC bus voltage. V_{dc}^{*} and V_{dc} are the reference voltage and actual voltage of DC bus of DSTATCOM respectively. K_{pd} and K_{id} are the proportional and integral gain of the PI controller over the DC bus voltage of DSTATCOM.

For voltage regulation, there might be phase difference (β) between the PCC voltages and supply currents corresponding to the required leading/ lagging supply currents to regulate the PCC voltage. Therefore, to regulate the voltage at PCC, this β can be estimated by using a PI controller over the amplitude of PCC voltage as:

$$\beta = K_{pa}V_e + K_{ia}\int V_e dt \quad (6)$$

where $V_e = V_t^{*} - V_t$ = error in PCC voltage. V_t^{*} and V_t are the reference voltage and actual voltage of PCC respectively. K_{pa} and K_{ia} are the proportional and integral gain of the PI controller over the PCC voltage. The amplitude of PCC voltage can be calculated as:

$$V_t = \sqrt{(2/3)\left(v_a^2 + v_b^2 + v_c^2\right)} \quad (7)$$

After solving eqns. (1),(3) and (4) the reference supply currents can be obtained as:

$$\begin{aligned} i_{sa}^{*} &= \left\{v_a - \left(v_b - v_c\right)\beta\right\}\left(p_{lavg} + p_{loss}\right)/A; \\ i_{sb}^{*} &= \left\{v_b - \left(v_c - v_a\right)\beta\right\}\left(p_{lavg} + p_{loss}\right)/A; \\ i_{sc}^{*} &= \left\{v_c - \left(v_a - v_b\right)\beta\right\}\left(p_{lavg} + p_{loss}\right)/A; \end{aligned} \quad (8)$$

where $A=\sum_{i=a,b,c} V^2 i$

These extracted reference supply currents (i_{sa}^{*}, i_{sb}^{*} and i_{sc}^{*}) are compared with the respective sensed supply currents (i_{sa}, i_{sb} and i_{sc}) and current errors after the amplification are used in the PWM current controller to generate the switching signals for the IGBTs of DSTATCOM.

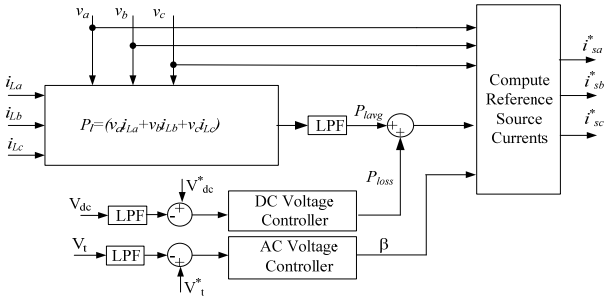


FIG. 2 BLOCK DIAGRAM OF EXTRACTING REFERENCE SUPPLY CURRENTS USING MODIFIED ISCT

Simulation Results and Discussion

The performance of DSTATCOM is studied with the proposed modified control algorithm. The DC bus voltage of DSTATCOM is selected to be 800 V for the supply voltage of 415V (L-L). To interface the VSC with the supply, the AC inductor of 2.3 mH is used. A DC capacitor of 8000 μF is used for self supporting DC bus of DSTATCOM. Initially considered linear load is 3-single phase load 15 kW, 0.8 pf lag and nonlinear load is a three single-phase rectifier with a DC resistive load of 10Ω and a capacitor of 400μF in parallel. The PCC voltage is considered 415 V (L-L), which has nearly 340 V per phase (amplitude). The simulations are carried out for both PFC mode and ZVR mode for the same conditions.

Performance of DSTATCOM in PFC Mode

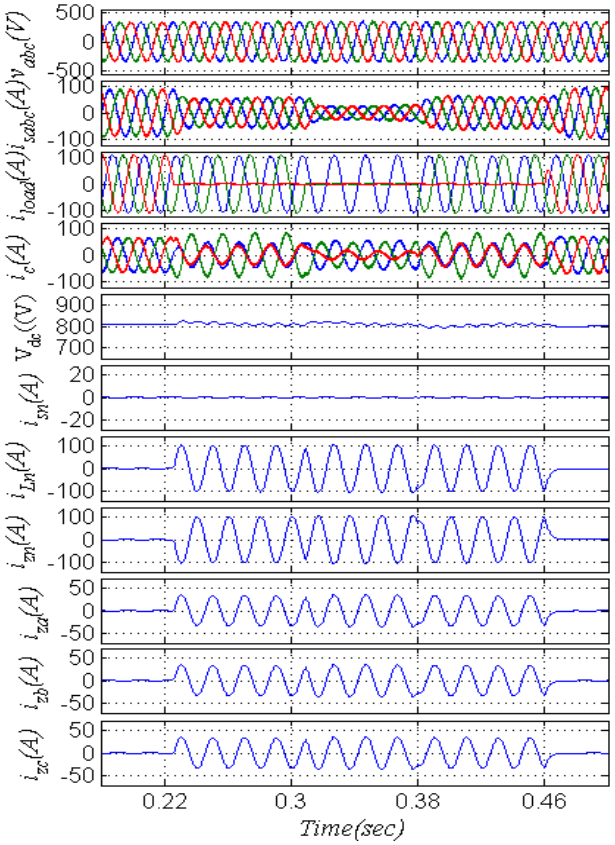


FIG. 3 PERFORMANCE OF DSTATCOM IN PFC MODE FOR LINEAR LOADS

The performance of DSTATCOM in PFC mode is shown in Fig. 3 and Fig. 4 for the power factor correction with load balancing, harmonics reduction and the neutral current compensation. The load of phase C is removed at t=0.22 s and again the load of phase B is removed at t=0.30 s. These loads are reapplied at t=0.38 s and t=0.46 s respectively. The PCC voltages (v_{abc}), supply currents (i_{sabc}), load currents (i_{Load}), compensator currents (i_c), DC bus voltage (V_{dc}),

supply neutral current (i_{sn}), load neutral current (i_{Ln}), neutral current of zigzag transformer (i_{zn}) and phase current of zigzag transformer (i_{za}, i_{zb} and i_{zc}) are shown in Fig. 3 with various loading conditions. It is observed that the supply currents are balanced and in phase of PCC voltages irrespective to loading conditions. The supply neutral current is reduced to few mA by providing the path through a zigzag transformer which compensates the load neutral current by splitting it equally among the three phases. The DC bus voltage of DSTATCOM is maintained at its reference voltage during different load conditions.

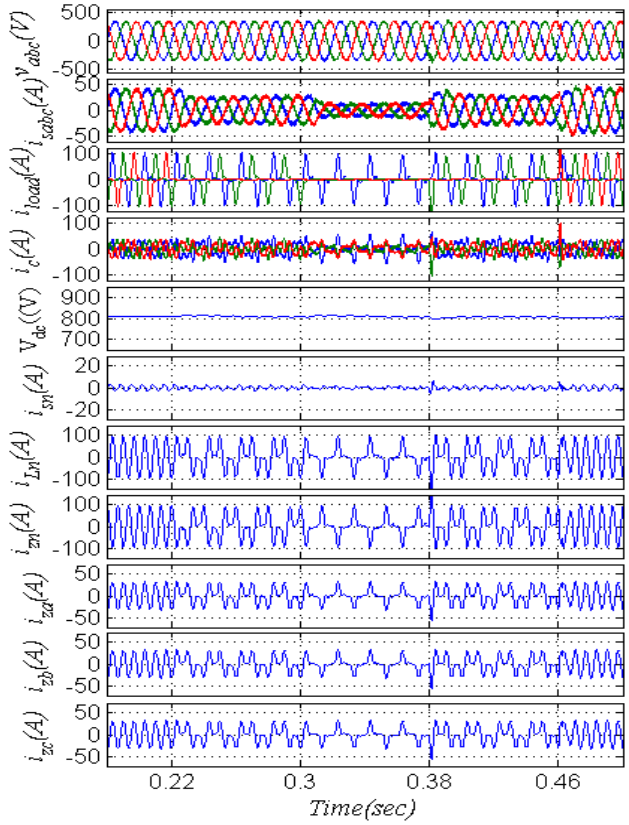


FIG. 4 PERFORMANCE OF DSTATCOM IN PFC MODE FOR NONLINEAR LOADS

The performance of the DSTATCOM for nonlinear loads under various loading conditions is shown in Fig. 4. The nonlinear loads are changed to two phase loads and to single phase load and applied back as in the case of linear loads. The supply currents are in phase of the PCC voltages as well as balanced and harmonics free even for unbalanced nonlinear loading conditions. The zigzag transformer reduces the supply neutral current to few mA. The DC bus voltage is also regulated to its reference value. The waveform, THD and spectra of the PCC voltage, supply current and load current are shown in Fig. 5. The THD of supply current is found 4.34% while that of load current is 84.35%.

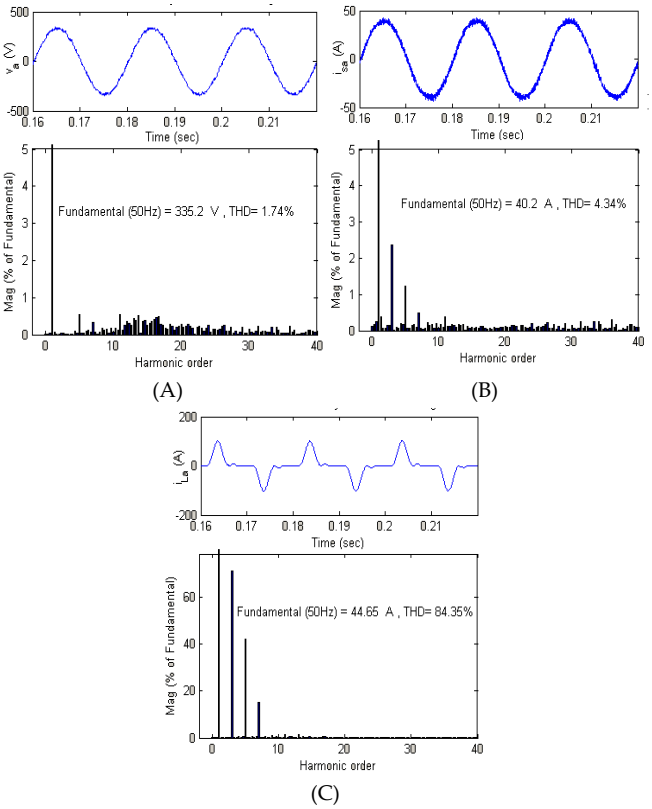


FIG. 5 WAVEFORM AND THD SPECTRUM OF (A)PCC VOLTAGE OF PHASE A (B)SUPPLY CURRENT OF PHASE A (C)LOAD CURRENT OF PHASE A IN PFC MODE.

Performance of DSTATCOM in ZVR Mode

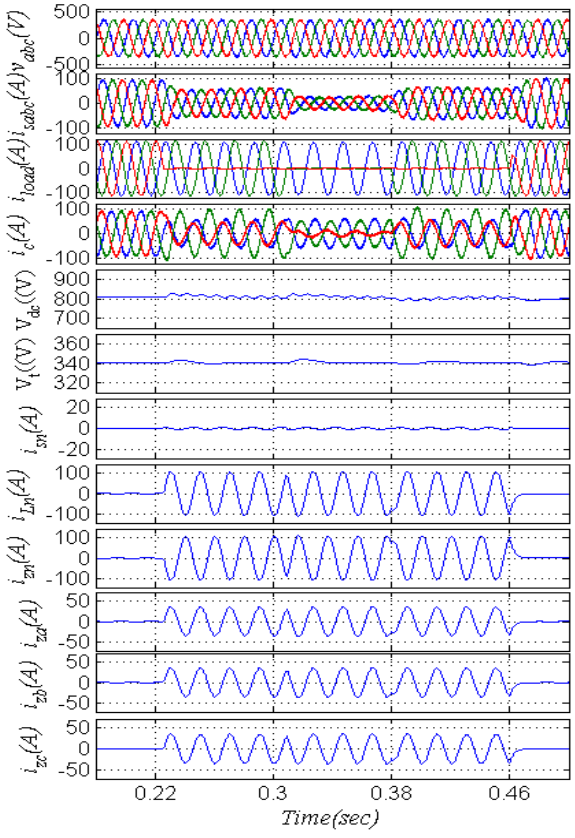


FIG. 6 PERFORMANCE OF DSTATCOM IN ZVR MODE FOR LINEAR LOADS.

The performance of DSTATCOM in ZVR mode is shown in Fig. 6 and Fig. 7. The load conditions in this mode are similar to PFC mode. It is observed that the supply currents are balanced by the DSTATCOM for the balanced and unbalanced linear loads with regulated DC bus voltage of DSTATCOM. The PCC voltage is regulated very close to its reference value for that the control algorithm has been modified. The supply neutral current is also reduced to few mA as shown in Fig. 6.

Fig. 7 shows the performance of DSTATCOM in ZVR mode for nonlinear loads. The supply currents are harmonics free and balanced. Voltage regulation is also achieved even with nonlinear unbalanced load by using of modified control algorithm. The DSTATCOM system compensates the load neutral current and reduces the supply neutral current to few mA. The DC bus voltage of DSTATCOM is also regulated to its reference voltage by the controller. The waveform, THD and spectra of the PCC voltage, supply current and load current in ZVR mode of DSTATCOM are shown in Fig. 8. The THD of supply current is found 3.96% while that of load current is 83.36%. Fig.5(A) and Fig. 8(A) show the PCC voltage with and without voltage regulation.

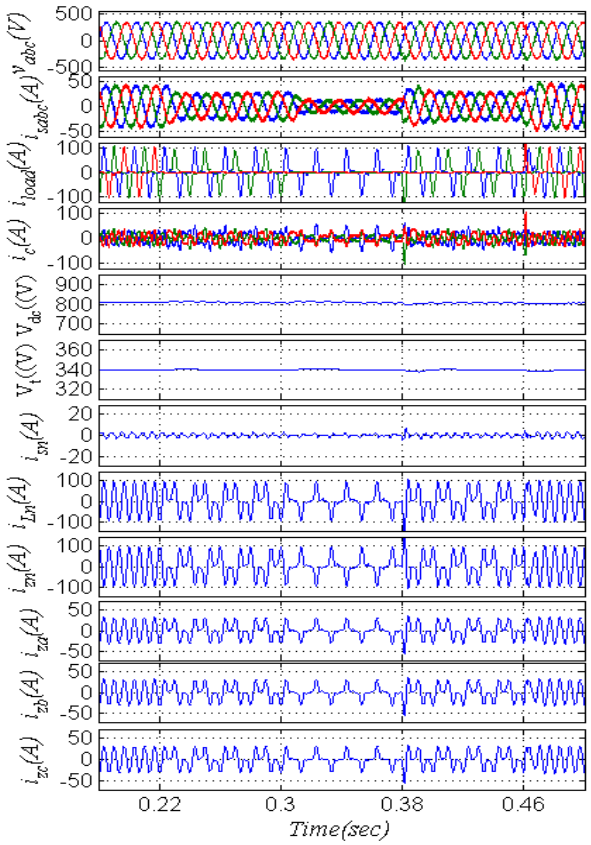


FIG. 7 PERFORMANCE OF DSTATCOM IN ZVR MODE FOR NONLINEAR LOADS.

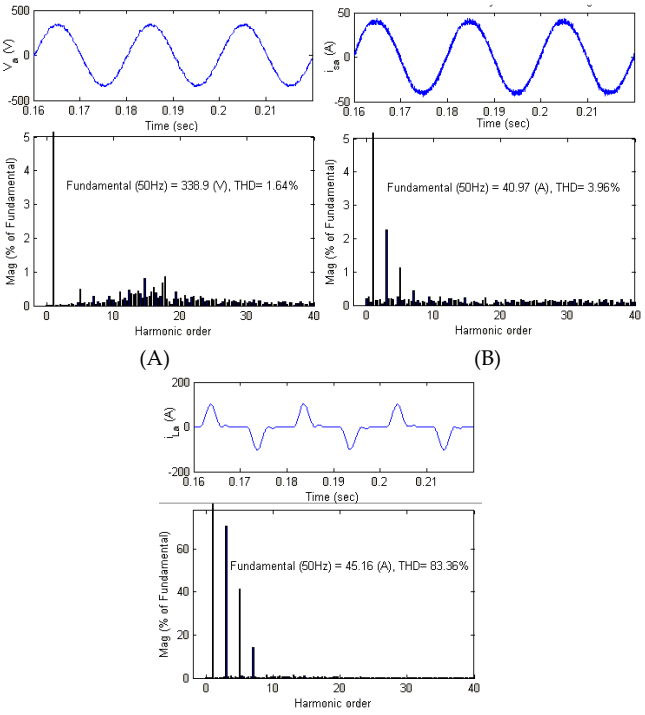


FIG. 8 WAVEFORM AND THD SPECTRUM OF (A)PCC VOLTAGE OF PHASE A (B)SUPPLY CURRENT OF PHASE A (C)LOAD CURRENT OF PHASE A IN ZVR MODE.

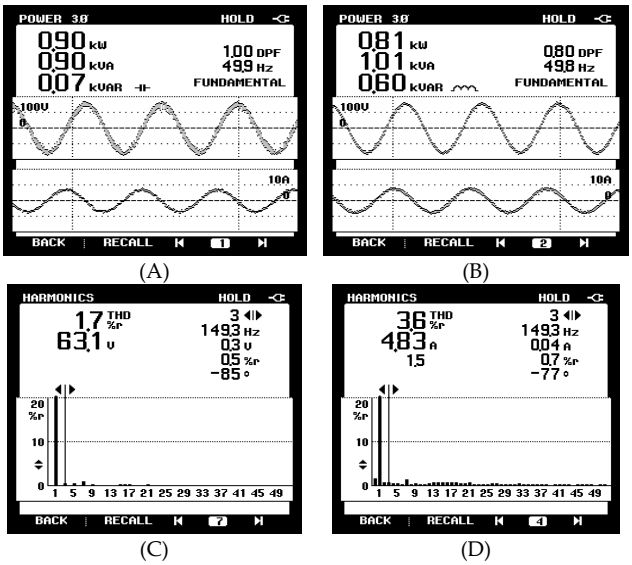
Experimental Validation

A prototype of the DSTATCOM is developed in the laboratory using the IGBTs based 'Semikron' made 3-leg VSC with a DC bus capacitor of 1650 μF and three single phase transformers of 2.5 kVA, 120V/120V are used to develop the zigzag transformer. The proposed DSTATCOM is connected to a 110 V, 50 Hz three phase supply system and tested for the various load conditions in the PFC mode. Five Hall effect current sensors and three Hall effect voltage sensors are used to get feedback signals (supply currents, load currents, PCC voltages and DC bus voltage) for controlling the DSTATCOM. The proposed modified control algorithm is implemented using the dSPACE DSP. A Fluke 43B power analyzer and a four channels Digital Storage Oscilloscope of Agilent Technologies make are used to record the tests results on the prototype. During experimental observations, DC bus voltage of DSTATCOM is regulated at 200 V and the prototype of DSTATCOM is tested for three different load conditions as discussed below.

Performance of DSTATCOM at Balanced 0.8 Lagging pf Linear Load

Figs. 9 (A) and (B) show the supply power and load power. The power factor on supply side is improved

to unity (Fig. 9(A)) while the power factor of load is 0.8 lagging (Fig. 9(B)) as the reactive power is compensated by the DSTATCOM. The waveform of supply current and load current of phase A are shown in Figs. 9 (A) and (B) respectively. The magnitudes of supply currents and load currents are given in Table 1. Figs. 9 (C) and (D) show that THD of PCC voltage of phase A is 1.7% and that of supply current of phase A is 3.6% in steady state. THD of three phase PCC voltages and supply currents load are given in Table 2. These results demonstrate the satisfactory steady state performance of the DSTATCOM system.



(A) (B)

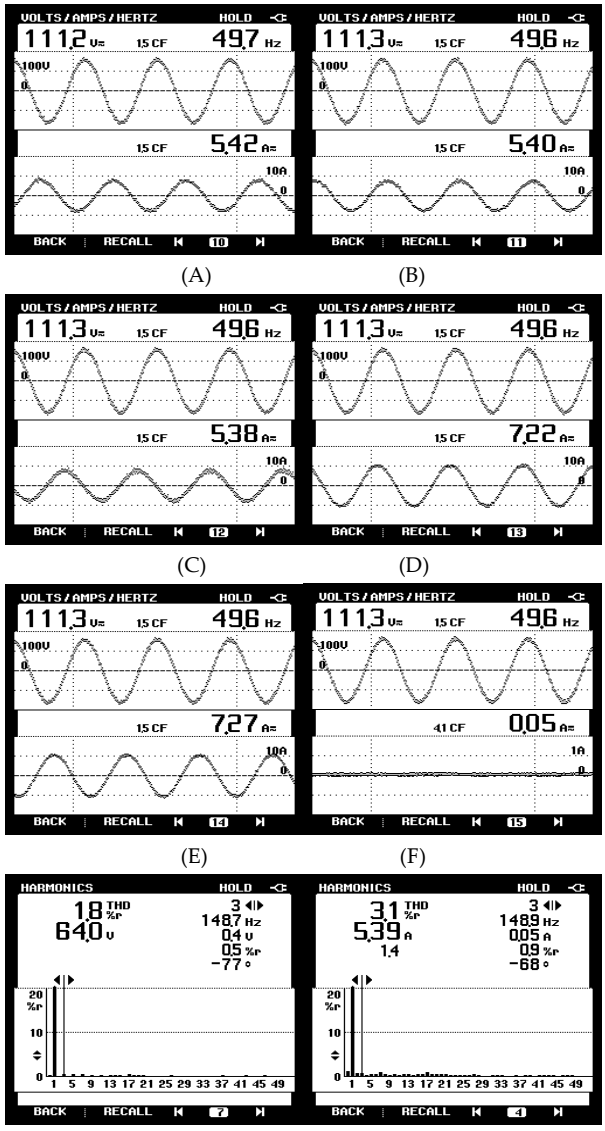
(C) (D)

FIG. 9 TEST RESULTS FOR BALANCED 0.8 LAGGING POWER FACTOR LOAD (A)SUPPLY POWER AND SUPPLY POWER FACTOR (B)LOAD POWER AND LOAD POWER FACTOR (C)PCC VOLTAGE THD OF PHASE A (D) SUPPLY CURRENT THD OF PHASE A

TABLE 1 VOLTAGES AND CUURENTS OF OVERALL SYSTEM IN THREE PHASE UNDER DIFFERENT LOAD CONDITIONS

Compensation		Power factor correction	Load balancing	Harmonic rejection
Voltage at PCC (V)	AB	109.0	111.2	108.6
	BC	109.0	111.3	108.6
	CA	109.0	111.3	108.6
Supply current (A)	A	4.83	5.42	7.19
	B	4.84	5.40	7.18
	C	4.87	5.38	7.20
Load current (A)	A	5.17	7.22	7.23
	B	5.25	7.27	7.26
	C	5.32	0.00	7.27
Zigzag transformer current (A)	A	-	2.373	2.286
	B	-	2.343	2.279
	C	-	2.388	2.276
Neutral current (A)	Supply	0.00	0.096	0.173
	Load	0.00	7.16	6.93
	Zigzag transformer	0.00	7.15	6.91

Performance of DSTATCOM with Unbalanced Linear Load



(A) (B)

(C) (D)

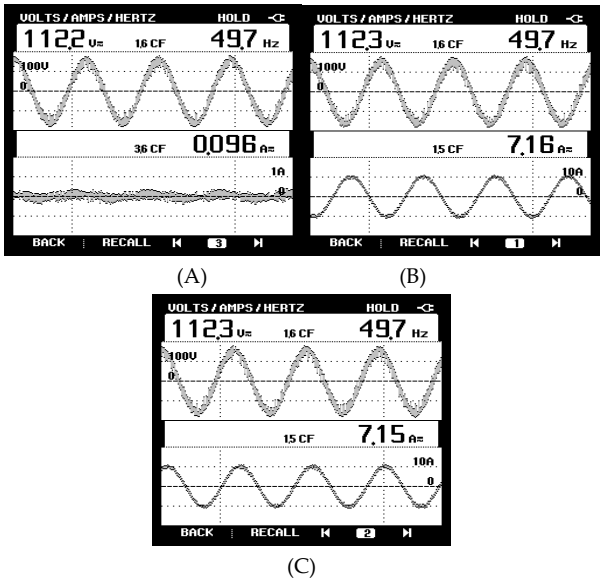
(E) (F)

(G) (H)

FIG. 10 TEST RESULTS FOR AN UNBALANCED LOAD (A) PCC VOLTAGE AND SUPPLY CURRENT OF PHASE A (B) PCC VOLTAGE AND SUPPLY CURRENT OF PHASE B (C) PCC VOLTAGE AND SUPPLY CURRENT OF PHASE C (D) PCC VOLTAGE AND LOAD CURRENT OF PHASE A (E) PCC VOLTAGE AND LOAD CURRENT OF PHASE B (F) PCC VOLTAGE AND LOAD CURRENT OF PHASE C (G) PCC VOLTAGE THD OF PHASE A (H) SUPPLY CURRENT THD OF PHASE A

Figs. 10 (A), (B) and (C) show three phase supply currents which are balanced while Figs. 10 (D)-(F) show load currents with one open phase (phase C) of load i.e. two phase loading of the system. The unbalanced load is compensated by DSTATCOM which is controlled by proposed algorithm and supply currents become equal and balanced. THD and harmonic spectra of PCC voltage and supply current of phase A are shown in Figs. 10 (G) and (H)

respectively. The voltage THD is found 1.8% and supply current THD is 3.1%. The zigzag transformer currents are given in Table 1. THD of PCC voltage and supply current of phase B and phase C are given in Table 2. It is observed when one phase of load is opened and load neutral current is 7.16A, the zigzag transformer reduces the supply neutral current to few mA as shown in Figs. 11 (A)-(C). These test results demonstrate performance of the DSTATCOM for the load balancing and neutral current with proposed algorithm.



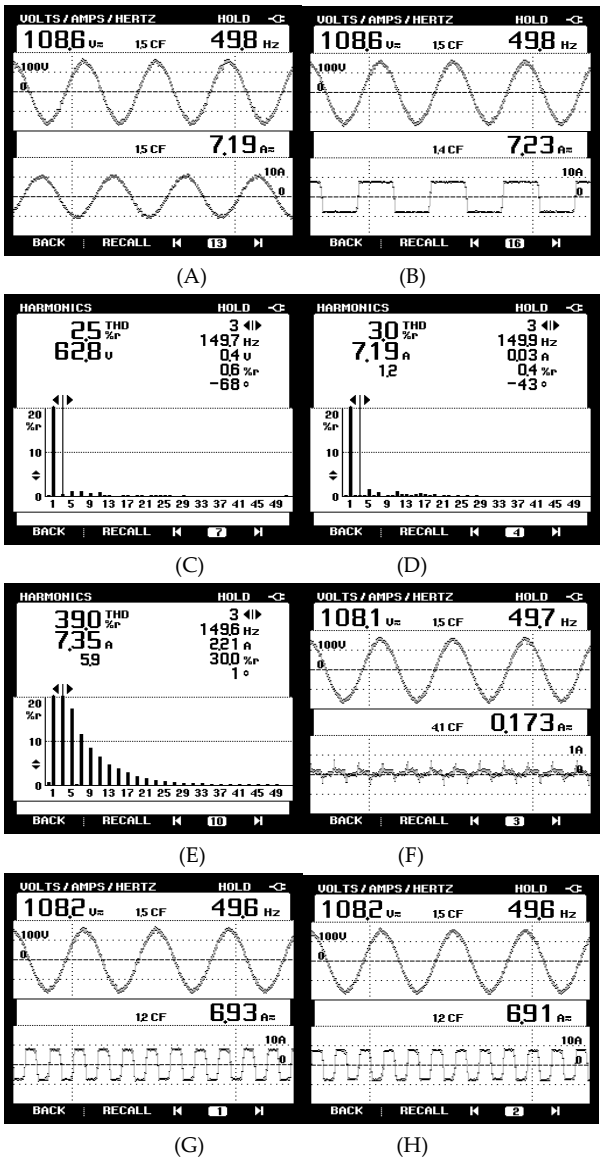
(A) (B)

(C)

FIG. 11 TEST RESULTS FOR AN UNBALANCED LOAD (A)PCC VOLTAGE AND SUPPLY NEUTRAL CURRENT (B)PCC VOLTAGE AND LOAD NEUTRAL CURRENT (C)PCC VOLTAGE AND ZIGZAG TRANSFORMER NEUTRAL CURRENT.

Performance of DSTATCOM at Nonlinear Load

The supply current and load current of phase A for the nonlinear load are shown in Figs. 12 (A) and (B), of which Fig. 12 (A) indicates that supply current is sinusoidal and harmonics free while Figs. 12 (B) shows the load current which is square wave. The nonlinear load is compensated by DSTATCOM to eliminate the current harmonics. Figs.12 (C)-(E) show the THD and harmonic spectra of PCC voltage, supply current and load current. The supply current THD is reduced to 3.0% while the load current THD is 39.0% without much effecting the PCC voltage as THD of PCC voltage is 2.5%. The load neutral current is compensated by the zigzag transformer. The supply neutral current is reduced to few mA while the load neutral current is 6.93A as shown in Fig 12(F) and Fig. 12(G). Three-phase currents of supply, load, zigzag transformer and neutrals are given in Table 1. THD of PCC voltages, supply currents and load currents are given in Table 2.



(A) (B)

(C) (D)

(E) (F)

(G) (H)

FIG. 12 TEST RESULTS FOR A NONLINEAR LOAD (A) PCC VOLTAGE AND SUPPLY CURRENT OF PHASE A (B) PCC VOLTAGE AND LOAD CURRENT OF PHASE A (C) PCC VOLTAGE THD OF PHASE A (D) SUPPLY CURRENT THD OF PHASE A (E) LOAD CURRENT THD OF PHASE A (F) PCC VOLTAGE AND SUPPLY NEUTRAL CURRENT (G) PCC VOLTAGE AND LOAD NEUTRAL CURRENT (H) PCC VOLTAGE AND ZIGZAG TRANSFORMER NEUTRAL CURRENT.

TABLE 2 THD OF PCC VOLTAGE, SUPPLY AND LOAD CUURENT IN THREE PHASE UNDER DIFFERENT LOAD CONDITIONS

Compensation		Power factor correction	Load balancing	Harmonic rejection
Voltage THD at PCC (%)	A	1.7	1.8	2.5
	B	1.6	1.7	2.4
	C	2.3	2.1	3.1
Supply Current THD (%)	A	3.6	3.1	3.0
	B	3.3	2.9	2.9
	C	3.8	2.7	2.8
Load Current THD (%)	A	-	-	39.0
	B	-	-	38.9
	C	-	-	38.6

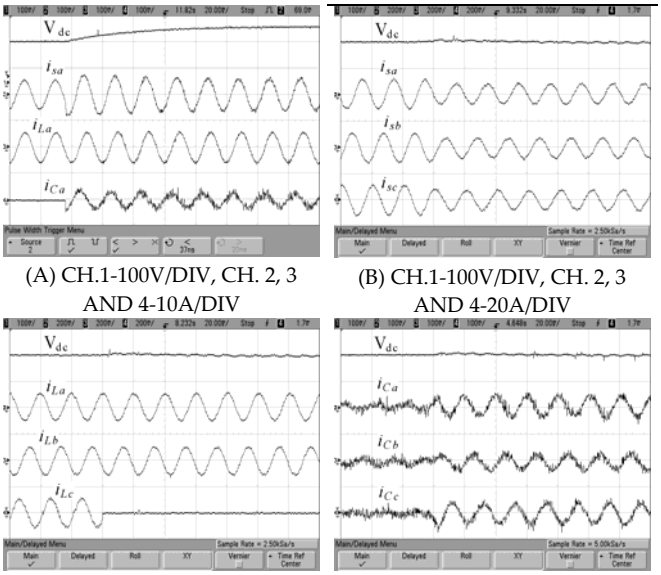
These test results demonstrate that supply currents are

harmonics free and supply neutral current is reduced to few mA for a nonlinear load by using DSTATCOM with proposed algorithm.

Dynamic Performance of DSTATCOM

The switch in response of the DSTATCOM for the compensation of 0.8 lagging pf load is shown in Fig.13(A). The DC bus voltage is regulated to its reference value of 200 V with the switch-in of DSTATCOM. The supply currents are reduced to active component of the load currents as the reactive power of load is compensated by the DSTATCOM.

Figs. 13 (B), (C) and (D) show supply currents, load currents and compensator currents with DC bus voltage at the instant of opening of one phase (phase C) of load. With the opening of one phase (phase C) of load, supply currents are balanced and DC bus voltage of DSTATCOM is regulated to its reference value of 200 V with a small fluctuation at the instant of opening of one phase.



(A) CH.1-100V/DIV, CH. 2, 3 AND 4-10A/DIV

(B) CH.1-100V/DIV, CH. 2, 3 AND 4-20A/DIV

(C) CH.1-100V/DIV, CH. 2, 3 AND 4-20A/DIV

(D) CH.1-100V/DIV, CH. 2, 3 AND 4-20A/DIV

FIG. 13 DYNAMIC PERFORMANCE OF DSTATCOM (A) DC BUS VOLTAGE, SUPPLY CURRENT, LOAD CURRENT AND DSTATCOM CURRENT OF PHASE A (B) DC BUS VOLTAGE AND THREE PHASE SUPPLY CURRENTS (C) DC BUS VOLTAGE AND THREE PHASE LOAD CURRENTS (D) DC BUS VOLTAGE AND THREE PHASE DSTATCOM CURRENTS

These results demonstrate the satisfactory performance of the algorithm to control the DSTATCOM.

Conclusion

The simulation and implementation of a DSTATCOM with the proposed modified algorithm based on instantaneous symmetrical component theory (ISCT) has been carried out for the load compensation as well as the neutral current compensation. The proposed algorithm is found effective to control the DSTATCOM for regulating the PCC voltage with the load balancing and harmonics elimination. The power factor correction and voltage regulation modes both have been achieved with proposed modified algorithm of DSTATCOM. The self-supporting DC bus of DSTATCOM has been found stable for the various loading conditions. The zigzag transformer has been found effective not only to compensate the fundamental and harmonic neutral currents but also to enhance the load balancing capability of proposed DSTATCOM by splitting the load neutral current equally among the three phases.

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Appendix

Data for Simulation

AC line voltage 415V (L-L), 50 Hz; supply impedance: R_s=0.1 Ω, L_s=2 mH; voltage supply converter: DC link voltage 800 V, DC capacitor 8000 μF, interfacing inductor 2.3 mH, switching frequency 10 kHz. For ripple filter: R_r =2Ω, C_r=20 μF; zigzag transformer: 3 single phase transformers 7.5 kVA, 240 V/240 V; linear load: star-connected 3-single phase load 15 kW, 0.8 pf lag, each; nonlinear load: star-connected 3 single phase rectifier with RC load R =10Ω, C=400 μF. K_{pd}=250, K_{id}=150, K_{pa}=0.015, K_{ia}=0.022.

Data for Hardware Implementation

AC line voltage 110 V, 50 Hz; VSC: DC bus voltage 200 V, DC bus capacitor 1650 μF, interfacing inductance 3 mH, maximum switching frequency 10 kHz, zigzag transformer: 3 single phase transformers 2.5 kVA, 120 V/120 V; 5-Hall effect current sensors (LEM CT-100S) and 3-Hall effect voltage sensors (LEM CV3-1500).